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ABSTRACT OF THE DISCLOSURE

The present invention relates to a shallow trench isolation method of a semiconductor wafer which fills dielectric material into shallow trenches between components on the surface of the semiconductor wafer to electrically isolate the components. This method can prevent dishing phenomenon from occurring over the surface of some wider shallow trenches when a chemical-mechanical polishing method is used to polish the surface of the dielectric material filled in each shallow trench. The method comprises: (1) choosing the shallow trenches with widths greater than a predetermined size and generating at least one dummy in each chosen shallow trench to form a plurality of new trenches with widths less than the predetermined size; (2) covering the surface of the semiconductor wafer with dielectric material to form a dielectric layer; (3) condensing the dielectric layer; (4) polishing the surface of the dielectric layer filled in all the shallow trenches to align the surface of the dielectric material with the surface of the components on the semiconductor wafer.